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(71) Applicant *(for all designated States except US)*: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **SANDULEANU, Mihai, A., T.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: **DUIJVESTIJN, Adrianus, J.**; Philips Intellectual Property & Standards, Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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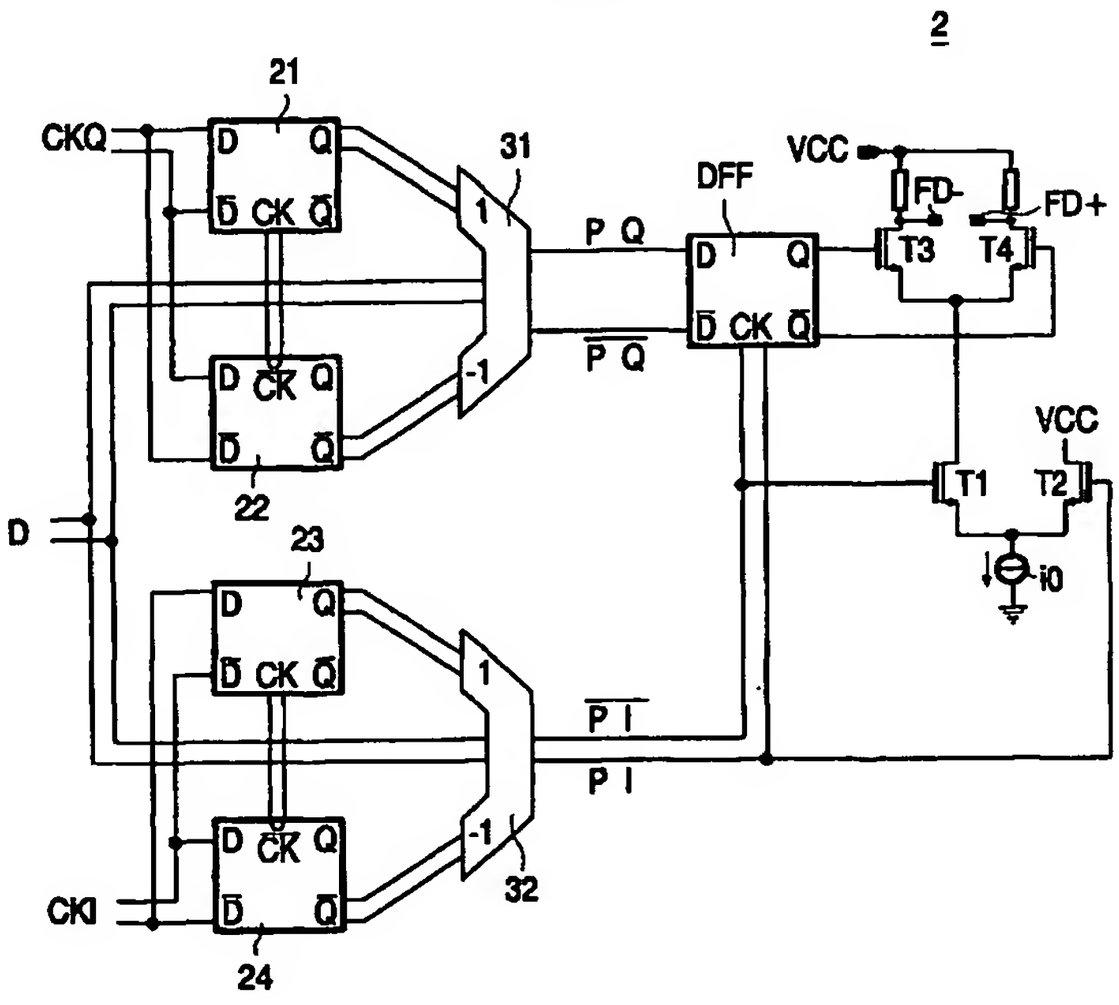
Declaration under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD,*

[Continued on next page]

(54) Title: PLL USING UNBALANCED QUADRICORRELATOR



(57) Abstract: A Phase Locked Loop (1) used in a data and clock recovery comprising a frequency detector (10) including a quadricorrelator (2), the quadricorrelator (2) comprising a frequency detector including double edge clocked bi-stable circuits (21, 22, 23, 24) coupled to a first multiplexer (31) and to a second multiplexer (32) being controlled by a signal having a same bitrate as the incoming signal (D), and a phase detector (DFF) controlled by a first signal pair (PQ, $\overline{PQ}$) provided by the first multiplexer (31) and by a second signal pair (PI, $\overline{PI}$) provided by the second multiplexer (32).

WO 2004/042927 A1

MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

PLL using unbalanced quadricorrelator

The invention relates to a Phase Locked Loop (PLL) comprising a frequency detector including an unbalanced quadricorrelator.

PLL circuits are widely used in modern communication circuits for tuning receivers. Normally a PLL comprises a voltage-controlled oscillator (VCO), a frequency control loop having a frequency detector and a phase control loop including a phase detector. When the incoming signal in the PLL is a high-speed Non Return to Zero (NRZ) random signal, phase detectors and frequency detectors have the difficult task to work on random transitions of the incoming signal. PLLs using NRZ signals are often called data and clock recovery circuits (DCR). Between transitions the phase and frequency detectors should maintain the phase error and frequency error information such that the voltage controlled oscillator is not pulled away from lock when transitions are missing.

A known implementation of the frequency detector is the quadricorrelator concept as in "Digital Logic Implementation of Quadricorrelators for Frequency detectors", by C. G . Yoon, S. Y. Lee and C. W. Lee, IEEE Proc. of 37th MidWest Symposium on Circuits and Systems, 1994, pp. 757 – 760. A model for an unbalanced digital quadricorrelator is an unbalanced analog quadricorrelator as shown in Fig. 1. The analog quadricorrelator comprises a first pair of mixers M1, M2 supplied by quadrature signals I, Q and input signal INP. Outputs of said pair of mixers M1, M2 are coupled to a pair of low-pass filters L1, L2, the filters providing signals Vi and Vq, respectively. The signal Vi is inputted to a derivation circuit D1. The signal Vq and the signal provided by the derivation circuit D1 are inputted to a third mixer M3, the mixer generating a signal FD, which is indicative for a frequency error between the input signal INP and quadrature signals I, Q. In the above-mentioned document a digital implementation of the analog balanced quadricorrelator, is presented. The digital implementation comprises single edge flip-flops coupled to a combinatorial network. Hence, the flip-flops detects only phase shifts between quadrature inputs and a rising edge of the D input signal, which means that this quadricorrelator works at half rate or 2* Tbit. Tbit is defined as the time period for a high or a low binary level.

Furthermore, the combinatorial part of the quadricorrelator comprises 6 AND gates and 2 OR gates that cause delays or, alternately, phase-shifts between the signals provided by the quadricorrelator.

It is therefore an object of this invention to mitigate at least some of the above mentioned problems.

In accordance with the invention this is achieved in a device as described in the first paragraph being characterized in that the quadricorrelator comprises a frequency detector including double edge clocked bi-stable circuits coupled to a first multiplexer and to a second multiplexer being controlled by a signal having a same bitrate as the incoming signal, and a phase detector controlled by a first signal pair provided by the first multiplexer and by a second signal pair provided by the second multiplexer. According to the invention, the input information is read on both the rising and falling edges of the clock signal, meaning that the input information is read every half period of the clock i.e. at Tbit rate. This feature could be implemented either having a direct coupling between the clock signal and bi-stable circuits or using intermediate signals obtained during processing input signal having the same Tbit. This means that bi-stable circuits could be combined with combinatorial circuits having a control input e.g. multiplexers for working at Tbit speed. Furthermore, the phase detector comprises a double edge bi-stable circuit and therefore it preserves the Tbit speed. It is further observed that a delay of a signal through one bi-stable circuit is expected to be less that a delay through three layers of combinatorial circuits as used in the prior-art.

In an embodiment of the invention the frequency detector comprises a first pair of double edge clocked bi-stable circuits coupled to the first multiplexer and a second pair of double edge clocked bi-stable circuits coupled to the second multiplexer, which first and second pairs are supplied by mutually quadrature phase shifted signals, respectively, to provide the first signal pair and the second signal pair indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals. The first multiplexer and the second multiplexer provide a first signal and a second signal indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals. The mutually quadrature phase shifted signals are generated by a voltage controlled oscillator. In many applications as optical networking a clock recovery is necessary especially when the clock information in missing from the input signal as in Non Return to Zero (NRZ) signals. Furthermore, clock recovery circuits, which are in fact PLLs having a

quadrature voltage-controlled oscillator providing quadrature signals i.e. mutually shifted with 45 degrees. PLLs also have a phase detector and a frequency detector. The outputs of the multiplexers are updated only on the transitions of the incoming signal maintaining the same error at the output between transitions. The phase difference between the incoming signal and quadrature clock signals is transformed in a positive or negative quantified signal. When this signal is positive the clock increases its phase and for negative signals, the clock decreases its phase.

In another embodiment of the invention the phase detector comprises a D flip-flop receiving the first signal pair and being clocked by the second signal pair, the second signal pair being inputted to respective gates of a first transistor pair for determining a state ON or OFF of a current through said first transistor pair. The current through the first transistor pair biases a second transistor pair, the second transistors pair receiving the first signal pair and generating an output signal indicative for a frequency error between the incoming data signal and Clock signals. According to the second signals pair, the current can flow in the source of the first transistors or can be dumped to Vcc. In equilibrium, a differential output of the frequency detector is zero.

The above and other features and advantages of the invention will be apparent from the following description of the exemplary embodiments of the invention with reference to the accompanying drawings, in which:

Fig. 1 depicts a prior art quadricorrelator,

Fig. 2 depicts a schematic diagram of digital quadricorrelator according to the invention,

Fig. 3 depicts rotating wheel analogy for mutually quadrature signals,

Fig. 4 depicts frequency detection algorithm, according to the invention, and

Fig. 5 depicts a PLL having a frequency detector as described in the present invention.

Fig. 2 depicts a schematic diagram of digital quadricorrelator according to the invention. The quadricorrelator 2 comprises double edge clocked bi-stable circuits 21, 22, 23, 24 coupled to multiplexers 31, 32 being controlled by a signal having the same bit rate as the incoming signal D. A first pair of double edge clocked bi-stable circuits 21, 22 coupled to a

first multiplexer 31 and a second pair of double edge clocked bi-stable circuits 23, 24 coupled to a second multiplexer 32 are supplied by mutually quadrature phase shifted signals CKQ and CKI respectively and providing a first pair of signals PQ, $\overline{PQ}$ and a second pair of signals PI, $\overline{PI}$ indicative for a phase difference between the incoming signal D and mutually quadrature phase shifted signals CKQ, CKI. It could be pointed out here that the bi-stable circuits could be flip-flops or latches. For the purpose of illustration in Fig. 2 is shown an implementation using D-type latches. The mutually quadrature signals are generated by a voltage controlled oscillator VCO, shown in Fig. 5.

The combination latch-multiplexer performs as a latch clocked on both transitions of the incoming signal D. The incoming signal D transitions are sampled by the two quadrature signals CKQ and CKI at Tbit rate. The outputs of the multiplexers are updated only on the incoming signal D transitions keeping the same error at the output between transitions. The second signal pair PI, $\overline{PI}$ is the output of the phase detector and the first pair of signals PQ, $\overline{PQ}$ is in quadrature with it. The phase difference between the incoming signal D and CKQ, respectively CKI is transformed in a positive or negative quantified signal. When this signal is positive the clock increases its phase and for negative signals, the clock decreases its phase. Let denote the first pair of signals PQ, $\overline{PQ}$ as Q and the second pair of signals PI, $\overline{PI}$ as I, and let us further observe that the signals I and Q are differential signals i.e. they are mutually shifted by substantially 180 degrees. The phase detector comprises a D flip-flop DFF receiving the first signal pair Q and being clocked by the second signal pair I. The second signals pair I is inputted to a first transistor pair T1, T2 respective gates for determining a state ON or OFF of a current I0 through said first transistors pair T1, T2. The current I0 is generated by a current source coupled to a common source node of the transistors T1, T2. The current I0 through the first transistor pair T1, T2 biases a second transistor pair T3, T4, the second transistor pair T3, T4 receiving the first signal pair Q and generating an output signal FD+, FD- indicative for a frequency error between the incoming data signal D and Clock signals CKI, CKQ. Let us denote the output signal FD+, FD- as FD. The algorithm can be visualized as shown in Fig. 4. Obviously the four possible cases will converge towards the equilibrium position. Table 1 presents the four situations and can be used to build the logic for the frequency detector.

As shown in Fig. 2, the second signal I is used to clock the D latch DFF, sampling the first signal Q. According to the I values, the current Io can flow in the source of the first transistor pair T1, T2 or can be dumped to Vcc. In equilibrium, when I is positive the

first transistor pair T1, T2 is not active any longer and the differential output FD of the frequency detector is zero. Now, only the phase detector contributes to the phase correction.

Table 1: Frequency detector logic

PD_I (I vector)	PD_Q (Q vector)	FD
-/+	-1	0
-/+	1	0
+/-	-1	-1
+/-	1	+1

The equilibrium position for the signals I and Q can be represented with the rotating wheel analogy as shown in Fig. 3. When it is a phase lock, the vector I is positive, stable and equal with +1 and the Q vector bounces from the positive to the negative quadrant in a periodic fashion. Frequency error generation signal for the frequency detector is explained with the aid of Fig. 4 and comprises the following steps:

- When I has a negative to positive transition for positive Q vectors, keep the frequency by generating a zero signal at the output of the frequency detector.

- When I has a negative to positive transition for negative Q vectors, keep the frequency by generating a zero signal at the output of the frequency detector.

When I has a positive to negative transition and Q is positive, increase the frequency (FD=+1)

- When I has a positive to negative transition and Q is negative, decrease the frequency (FD=-1).

When the clock is too slow as shown in Fig. 4, the pair of the two quadrature signals I and Q rotate counter-clockwise with an angular frequency equal to the frequency difference $\Delta\omega$ and the derivative of the signal I falling on top of Q signal generating an error signal.

When the clock is too fast, the pair of the two quadrature signals I and Q rotate clockwise with an angular frequency equal to the frequency difference $\Delta\omega$ and the derivative of the signal I falling in top of signal Q with 180° phase difference signal generating an error signal.

Fig. 5 depicts a PLL having a frequency detector 10 as described in the present invention. The error signal FD is inputted to a coarse control input C of the voltage controlled oscillator VCO via a first charge pump 20 coupled to a first low-pass filter 30 coupled to a second adder 80. The frequency error signal FD is inputted to the coarse input C of the VCO

because the VCO has to adapt as quickly as possible to frequency differences between the incoming signal D and the quadrature signals CKI and CKQ. A fine control input F of the VCO is controlled by a signal PD provided by a phase detector 70 coupled to a second charge pump 60 coupled to second low-pass filter 50.

Once the frequency lock is acquired the output of the frequency detector provides a zero DC signal at the output such that the VCO keeps the frequency information.

It is remarked that the scope of protection of the invention is not restricted to the embodiments described herein. Neither is the scope of protection of the invention restricted by the reference numerals in the claims. The word 'comprising' does not exclude other parts than those mentioned in the claims. The word 'a(n)' preceding an element does not exclude a plurality of those elements. Means forming part of the invention may both be implemented in the form of dedicated hardware or in the form of a programmed purpose processor. The invention resides in each new feature or combination of features. Throughout the description it was assumed that the signals I, Q and F are binary signals having an ON state represented by a +1 value and an OFF state represented by a –1 value.

CLAIMS:

1. A Phase Locked Loop comprising a frequency detector including an unbalanced quadricorrelator, the quadricorrelator comprising a frequency detector including double edge clocked bi-stable circuits coupled to a first multiplexer and to a second multiplexer being controlled by a signal having a same bitrate as the incoming signal, and a phase detector controlled by a first signal pair provided by the first multiplexer and by a second signal pair provided by the second multiplexer.

2. A Phase Locked Loop as claimed in claim 1, wherein the frequency detector comprises a first pair of double edge clocked bi-stable circuits coupled to the first multiplexer, and a second pair of double edge clocked bi-stable circuits coupled to the second multiplexer, which first and second pairs are supplied by mutually quadrature phase shifted signals respectively to provide the first signal pair and the second signal pair indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals.

3. A Phase Locked Loop as claimed in claim 1, wherein the phase detector comprises a D flip-flop receiving the first signal pair and being clocked by the second signal pair, the second signal pair being inputted to respective gates of a first transistors pair for determining a state ON or OFF of a current through said first transistors pair.

4. A Phase Locked Loop as claimed in claim 3, wherein current through the first transistor pair biases a second transistor pair, the second transistor pair receiving the first signal pair and generating an output signal indicative for a frequency error between the incoming data signal and Clock signals.

5. A Phase Locked Loop as claimed in claim 2, wherein the mutually quadrature phase shifted signals are generated by a voltage controlled oscillator.

6. A Phase Locked Loop as claimed in 5, wherein the error signal is inputted to a coarse control input of the voltage controlled oscillator via a first charge pump coupled to a first low-pass filter coupled to an adder.

7. A Phase Locked Loop as claimed in claim 6, wherein a fine control input is controlled by a signal provided by a phase detector coupled to a second charge pump coupled to second low-pass filter.

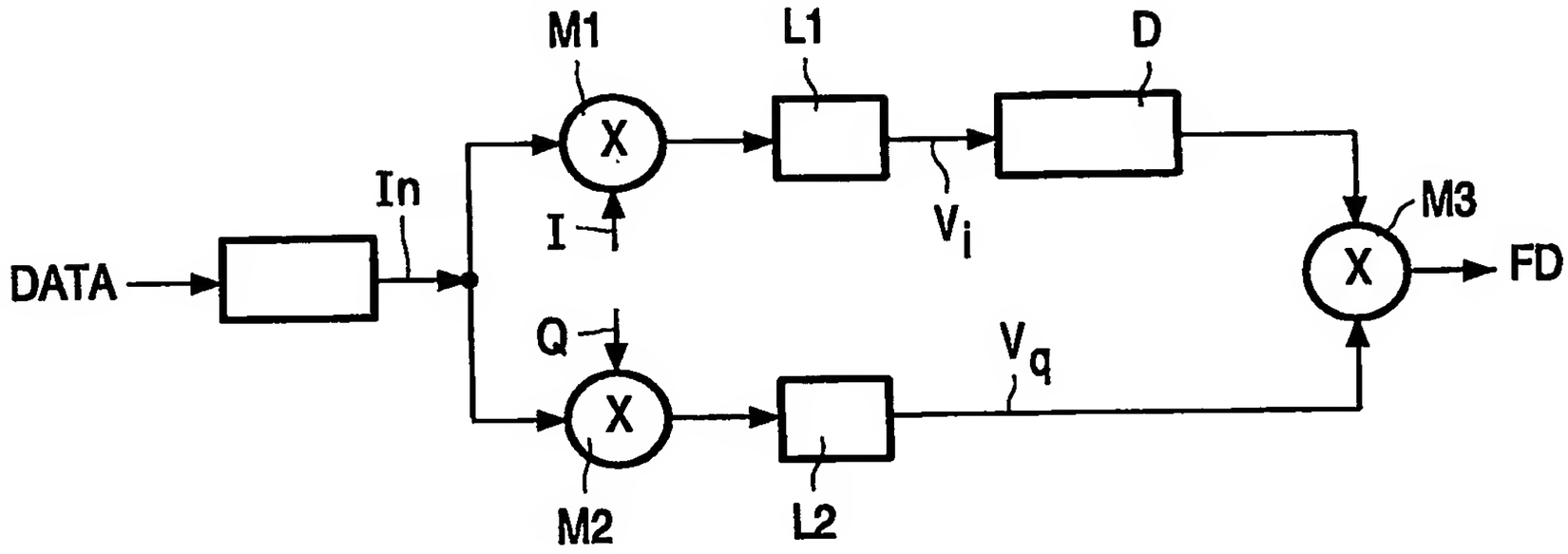
M1
L1
D
In
X
I
V_i
M3
DATA
X
FD
Q
V_q
X
M2
L2

FIG. 1

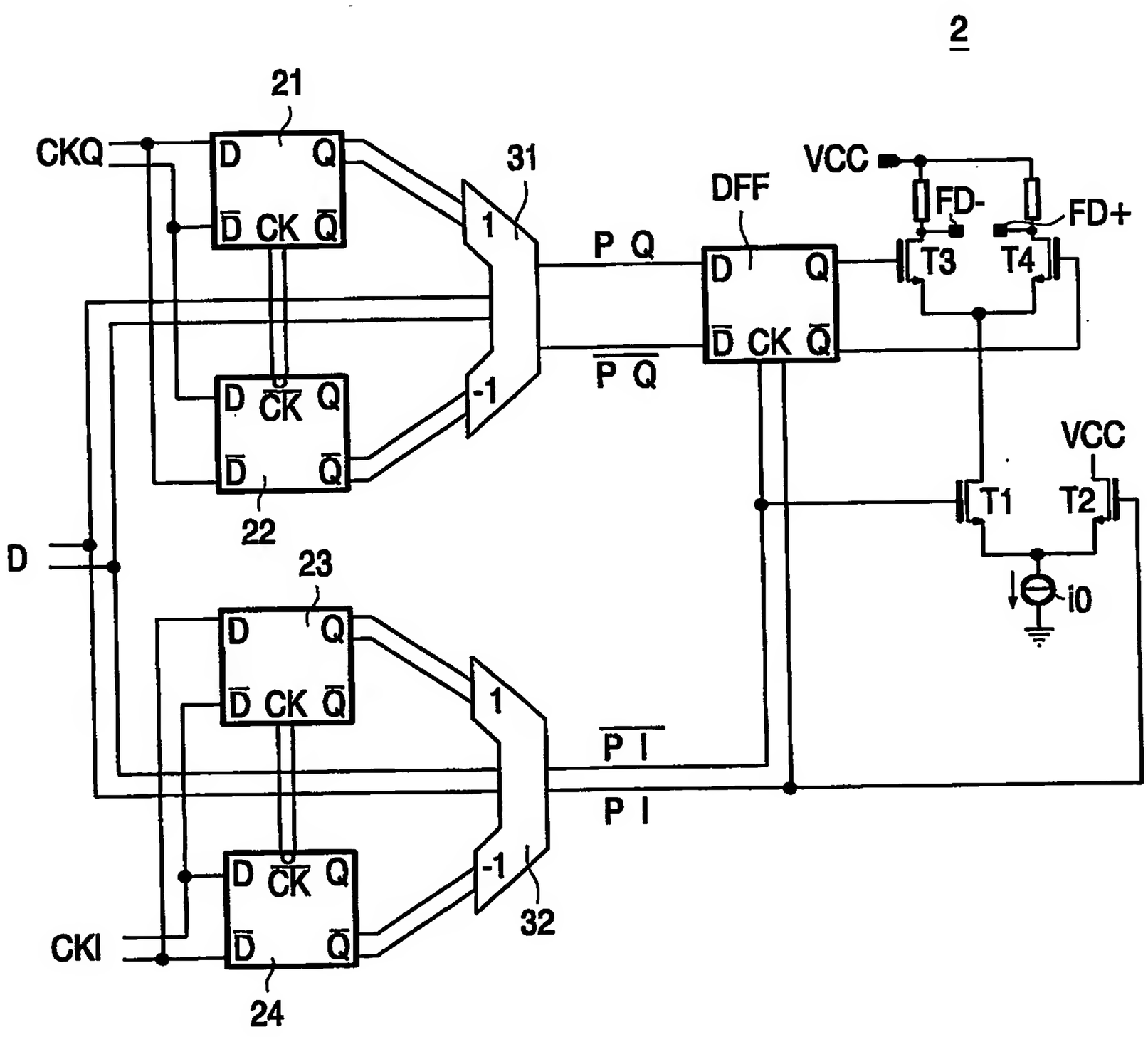
2
21
CKQ
D Q
D CK Q
31
1
P Q
DFF
VCC
FD-
FD+
T3
T4
D CK Q
-1
P Q
D CK Q
D Q
22
VCC
T1
T2
D
23
D Q
D CK Q
1
P I
i0
P I
D CK Q
-1
32
CKI
D Q
24

FIG. 2

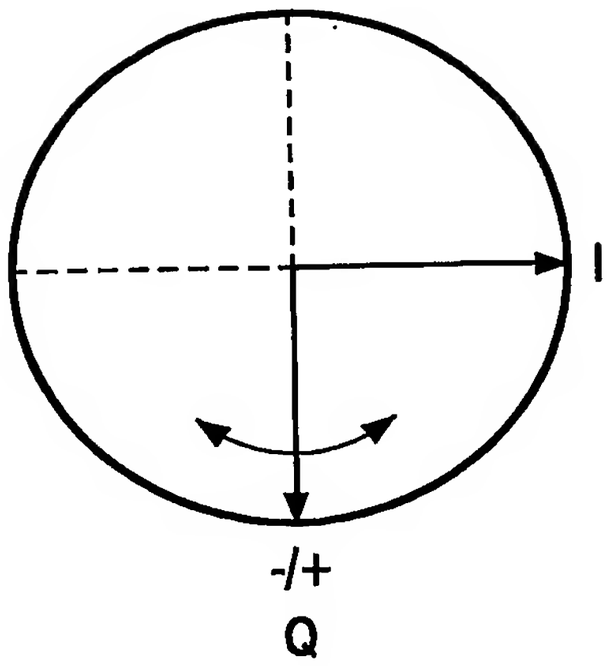

FIG. 3

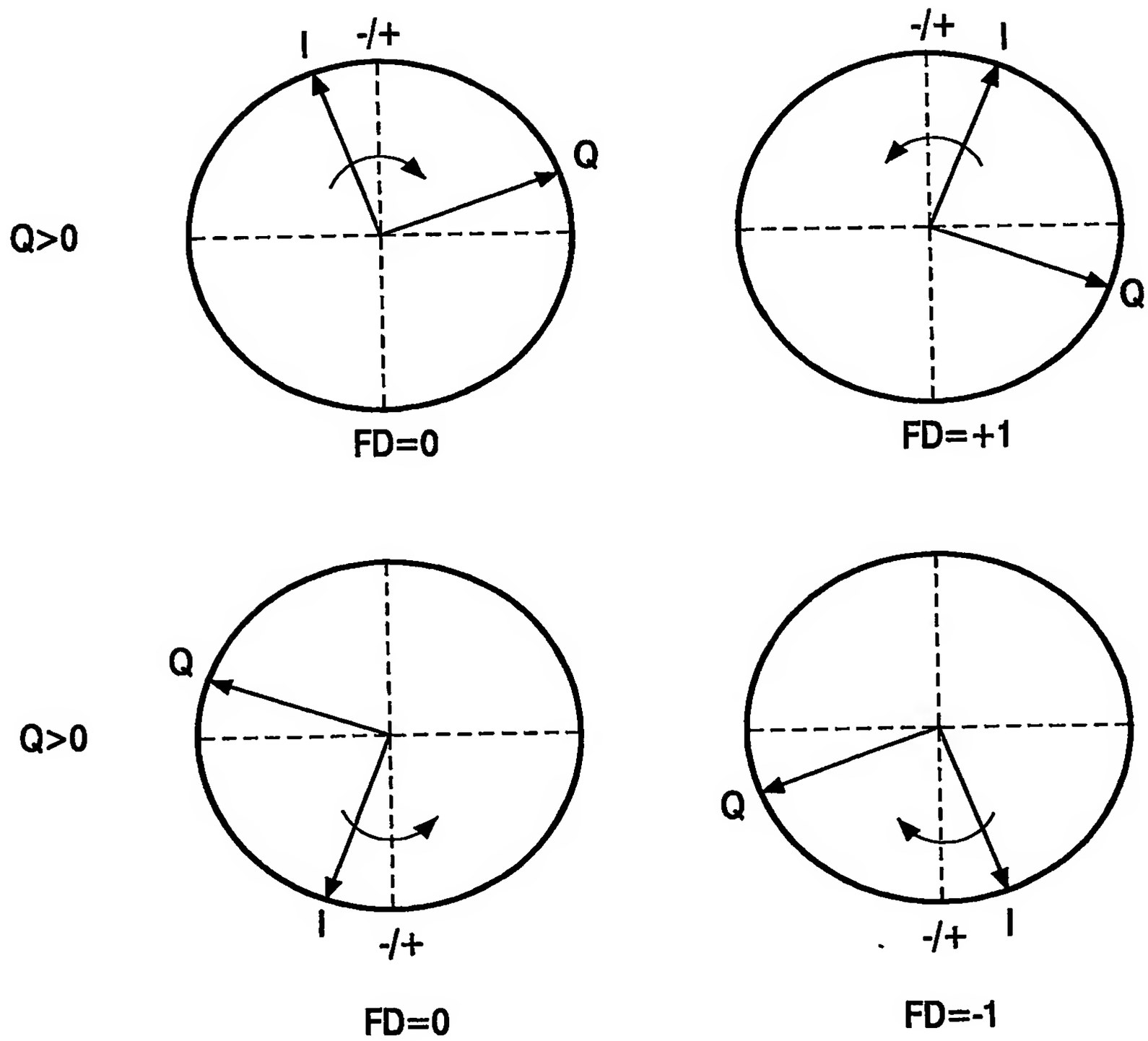

FIG. 4

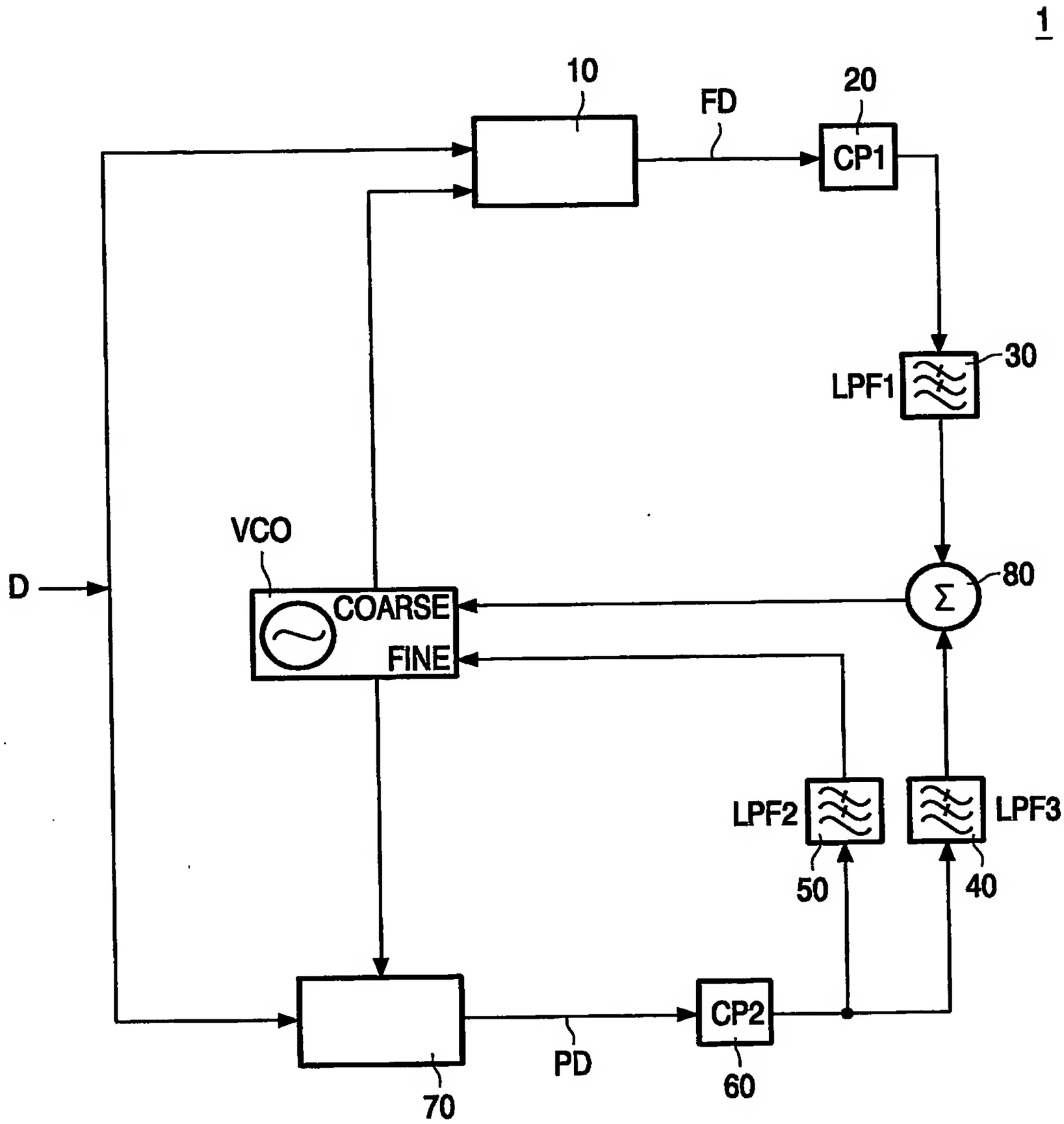
1
10
FD
20
CP1
LPF1
30
VCO
D
COARSE
FINE
80
Σ
LPF2
LPF3
50
40
CP2
PD
60
70

FIG. 5

INTERNATIONAL SEARCH REPORT

Intern[redacted]on No
PCT/I[redacted]03/04462

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03L7/091 H03L7/087

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03L H03D H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JAFAR SAVOJ ET AL: "Design of Half-Rate Clock and Data Recovery Circuits for Optical Communication Systems" PROCEEDINGS OF THE 38TH. ANNUAL DESIGN AUTOMATION CONFERENCE. (DAC). LAS VEGAS, NV, JUNE 18 - 22, 2001, PROCEEDINGS OF THE DESIGN AUTOMATION CONFERENCE, NEW YORK, NY: ACM, US, vol. CONF. 38, 18 June 2001 (2001-06-18), pages 121-126, XP002248306 ISBN: 1-58113-297-2 *section 2.1 Architecture* *section 3.2.2 Phase Detector* *section 3.2.3 Frequency Detector* --- -/--	1-7

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 February 2004	25/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Aouichi, M

INTERNATIONAL SEARCH REPORT

Inte[redacted]tion No
PCT/[redacted]03/04462

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 757 857 A (BUCHWALD AARON W) 26 May 1998 (1998-05-26) column 6, line 62 -column 7, line 38 column 10, line 3 -column 12, line 16 column 14, line 16 - line 35 figures 3,4	1-7

INTERNATIONAL SEARCH REPORT

Inter[redacted]tion No
PCT/[redacted] 03/04462

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5757857 A	26-05-1998	WO 9603800 A1	08-02-1996
		CA 2171734 A1	08-02-1996